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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/824,577	04/14/2004	Chia-Chen Liu	252011-2230	6533

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EXAMINER	
PERKINS, PAMELA E	
ART UNIT	**PAPER NUMBER**
2822	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/11/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/824,577	LIU ET AL.	
	Examiner	Art Unit	
	Pamela E. Perkins	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 December 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19,26 and 27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19,26 and 27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the filing of the RCE on 12 December 2006. Claims 1-19, 26 and 27 are pending.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-19, 26 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Johnson (6,525,953) in view Chakrabarti et al. (5,747,135) and Brask (2004/0188387).

Referring to claims 1, 14, 26 and 27, Johnson discloses a method of fabricating a semiconductor memory device where a first conductive layer (114), a first type doped semiconductor layer (130), a first dielectric layer (131), and a second type doped semiconductor layer (132) are sequentially formed on a substrate (100); patterning the second type doped semiconductor layer (132), the first dielectric layer (131), the first type doped semiconductor layer (130), and the conductive layer (114) along the first direction, thereby turning the conductive layer into a first conductive line; etching the second type doped semiconductor layer (132), the first dielectric layer (131), and the first type doped semiconductor layer (130) into a memory cell; depositing a second dielectric layer (not shown) overlying the substrate (100); planarizing the second

dielectric layer to expose the memory cell; and forming a second conductive line (123) overlying the second dielectric layer, running generally perpendicular to the first conductive line (Fig. 7; col. 8, line 36 thru col. 9, line 22; col. 11, lines 18-43).

Johnson does not disclose employing oxygen plasma sputtering to clean the substrate before deposition of a layer.

Chakrabarti et al. disclose a method of fabricating a semiconductor memory device where a layer (16) is formed over a substrate (12), wherein oxygen plasma sputtering is employed to clean the substrate before deposition of the layer (col. 3, lines 21-37).

Since Johnson and Chakrabarti et al. are both from the same field of endeavor, a method of fabricating a semiconductor memory device, the purpose disclosed by Chakrabarti et al. would have been recognized in the pertinent art of Johnson. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Johnson by employing oxygen plasma sputtering to clean the substrate before deposition of a layer as taught by Chakrabarti et al. to contaminants form the substrate (col. 3, lines 37-43).

Brask discloses a method of fabricating a semiconductor device where a semiconductor layer is etched thereby forming silicon residue on a surface; the surface is exposed to an oxidizing agent thereby removing the silicon residue (para. 2 & 10).

Since Johnson and Brask are both from the same field of endeavor, a method of fabricating a semiconductor device, the purpose disclosed by Brask would have been recognized in the pertinent art of Johnson. Therefore, it would have been obvious to

one of ordinary skill in the art at the time the invention was made to modify Johnson by etching a semiconductor layer thereby forming silicon residue on a surface and exposing the surface to an oxidizing agent thereby removing the silicon residue as taught by Brask. It is commonly known in the art that silicon residue can be formed on the surface after an etching process, this residue interferes that the intended dimensions of device features (para. 10).

Referring to claim 2 and 14, Johnson discloses the first type doped semiconductor layer as a p+ -type doped silicon layer (col. 11, lines 18-43).

Referring to claims 3 and 14, Johnson discloses the first conductive layer comprising a stack of TiN/TiSi2/p+-type doped silicon layers (col. 8, lines 45-53).

Referring to claims 4 and 14, Johnson discloses the first conductive line as a word line (Fig. 1; col. 4, lines 60-63).

Referring to claims 5 and 15, Johnson discloses the formation of the first dielectric layer comprises rapid thermal oxidation of silicon (col. 8, lines 61-67).

Referring to claims 6 and 14, Johnson discloses the second type doped silicon layer is n-type doped silicon layer (col. 11, lines 18-43).

Referring to claims 7 and 14, Johnson discloses the memory cell comprises a stack of p+-type doped silicon/first dielectric/n-type doped silicon layers (Fig. 7; col. 11, lines 18-43).

Referring to claims 12 and 14, Johnson discloses the second conductive layer comprises a stack of n+-type doped silicon/TiN/TiS_2/n+-type doped silicon/n-type doped silicon layers (Fig. 7; col. 11, lines 18-43).

Referring to claim s13 and 14, Johnson disclose the second conductive line as a bit line (Fig. 1; col. 4, lines 60-63).

Referring to claims 8-11 and 16-19, Chakrabarti et al. do not disclose a flow rate between 200 and 400sccm, a temperature between 225 and 275 ^{o}C and power between 1000 and 1500W. It would have been obvious to one having ordinary skill in the art at the time invention was made to perform oxygen plasma cleaning at a flow rate between 200 and 400sccm, a temperature between 225 and 275 ^{o}C and power between 1000 and 1500W disclosed in the claimed invention, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233 (CCPA 1955).

Response to Arguments

Applicant's arguments filed 12 December 2006 have been fully considered but they are not persuasive. As stated above, Johnson in view of Chakrabarti et al. and Brask disclose the method of fabricating a semiconductor memory device as described in independent claims 1 and 14.

In response to the applicant's arguments, the applicant argues prior art does not teach etching the second type doped semiconductor layer, the first dielectric layer, and the first type doped semiconductor layer into a memory cell causing particulate silicon residues on the surface of the first conductive line; depositing a second dielectric layer overlying the substrate, wherein oxygen plasma sputtering is employed to oxidize and

remove the particulate silicon residues on the surface of the first conductive line before deposition. Johnson discloses the claimed invention, including a second dielectric layer, except for the oxygen plasma sputtering employed to clean the substrate. The examiner is relying of the Chakrabarti et al. reference to teach oxygen plasma sputtering employed to clean the substrate. Cleaning a substrate after a patterning step is standard practice in the semiconductor field to remove residue. Also, Brask discloses etching a semiconductor layer thereby forming silicon residue on a surface and exposing the surface to an oxidizing agent thereby removing the silicon residue (para. 2 and 10).

Applicant has added the subjective intent of the method into the claim language, this does not further limit the scope of the claims.

"[T]he PTO can require an applicant to prove that the prior art products do not necessarily or inherently possess the characteristics of his claimed product. Whether the rejection is based on 'inherency ' under 35 U.S.C. 102, on 'prima facie obviousness' under 35 U.S.C. 103, jointly or alternatively, the burden of proof is the same." *In re Best 562 F.2d 1252, 1255, 195 USPQ 430, 433-34 (CCPA 1997).* "[W]here the Patent Office has reason to believe that a functional limitation assert to be critical for establishing novelty in claimed subject matter may, in fact, be an inherent characteristic of the prior art, it possesses the authority to require the applicant to prove that the subject matter shown to be in the prior art does not possess the characteristic relied on." *In re Best, supra 125455, 195 USPQ at 433* (quoting from *In re Swinehart, 58 CCPA 1027, 439 F.2d 210, 169 USPQ 226 (1971)*).

"In the first place, it is elementary that the mere recitation of a newly discovered function or property, inherently possessed by things in the prior art, does not cause a claim drawn to those things to distinguish over the prior art. Additionally, where the Patent Office has reason to believe that a functional limitation asserted to be critical for establishing novelty in the claimed subject matter may, in fact, be an inherent characteristic of the prior art, it possesses the authority to require the applicant to prove that the subject matter shown to be in the prior art does not possess the characteristic relied on." *In re Swinehart, supra. 169 USPQ at 229.*

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pamela E. Perkins whose telephone number is (571) 272-1840. The examiner can normally be reached on Monday thru Friday, 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on (571) 272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

PEP
7 January 2007

Zandra V. Smith
Supervisory Patent Examiner
7 Jan. 2007